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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,528	12/29/2000	Leslie E. Cline	42390P10231	8822

8791 7590 11/04/2003

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EXAMINER	
CHUNG, CHI WHAN	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 11/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,528	CLINE ET AL.	
	Examiner	Art Unit	
	Chi Whan Chung	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4 – 6, 9, 12 – 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Dischler et al., patent no. 6,311,287.

3. As per claim 1, **Dischler et al.** teach an apparatus comprising:

a table containing a plurality of entries, each including a frequency field and a voltage field [see Fig. 7 and col. 7 lines 60 – 65]; and

a register coupled to the table and having a selection field to select one of the plurality of entries [see Fig. 1, Fig. 2, Fig. 5B, col. 6 lines 12 – 19, col. 7 lines 18 – 24].

4. As per claim 4, Dischler et al. teach an apparatus, wherein the frequency field includes a processor clock frequency indicator [see Fig. 7 and col. 7 lines 60 – 65].

5. As per claim 5, Dischler et al. teach an apparatus, wherein the processor clock frequency indicator is a multiplier to be used with a phase locked loop circuit to generate a processor clock frequency [see Fig. 2, col. 7 lines 17 – 24, and col. 4 lines 45 – 56].

6. As per claim 6, Dischler et al. teach an apparatus, wherein the voltage field includes a processor operating voltage identifier [see Fig. 7 and col. 7 lines 47 – 59].

7. As per claim 9, Dischler et al. teach a computer system, comprising:

a clock generator to selectively output a clock signal at any of a plurality of selectable processor clock frequencies [Fig. 2 and col. 8 lines 13 – 19];

a power supply to selectively output any of a plurality of selectable processor operating voltages [col. 9 lines1 – 16];

a table coupled to the clock generator and the power supply and containing a plurality of entries, each entry including a frequency field and a voltage field [see Fig. 1, Fig. 7 and col. 7 lines 60 – 65]; and

a register coupled to the table and having a selection field to select one of the plurality of entries [see Fig. 1, Fig. 2, Fig. 5B, col. 6 lines 12 – 19, col. 7 lines 18 – 24].

8. As per claim 12, Dischler et al. teach a computer sytem, wherein the frequency field includes a processor clock frequency indicator [see Fig. 7 and col. 7 lines 60 – 65].

9. As per claim 13, Dischler et al. teach a computer system, wherein the processor clock frequency indicator is a multiplier to be used with a phase locked loop circuit to generate a processor clock frequency [see Fig. 2, col. 7 lines 17 – 24, and col. 4 lines 45 – 56].

10. As per claim 14, Dischler et al. teach a computer system, wherein the voltage field includes a processor operating voltage identifier [see Fig. 7 and col. 7 lines 47 – 59].

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2 –3, 7 – 8, 10 – 11, 15 – 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dischler et al., patent no.6,311,287, and Clark et al., patent no. 6,425,086.

13. As per claim 2, Dischler et al. teach an apparatus comprising means for selecting the minimum and maximum operable values of clock frequency [col. 8 lines 37 – 43]. Dischler et al. also teach a table containing a plurality of entries to store the maximum and minimum values of clock frequency and the values in between [see Fig. 7 and col. 7 lines 60 – 65]. Thus, Dischler et al. teach a table with selectable entries.

Dischler et al. do not teach a register that has a limit field to specify how many entries are selectable.

However, it is well known in the art to count the entries from a table and record the number in a register.

Therefore, it would have been obvious to one ordinary skilled in the art at the time the invention was made to read the number of selectable entries from Dischler et al.'s table and record the number value in a register so that the value could indicate a limit field to specify how many entries are selectable.

14. As per claim 3, Dischler et al. teach all of claim 1 and 2.

It is well known in the art to set some of the field in a register as read-write field, and to set some other field as read-only field.

Therefore, it would have been obvious to one ordinary skilled in the art at the time the invention was made to set the selection field in the register as a read-write field so that it would be possible to select different entries in the table, and to set the limit field as read-only field so that the choice of selectable entries would be fixed once set by the manufacturer in order to ensure safe performance of the processor.

15. As per claim 7, **Clark et al.** teach an apparatus, wherein a non-volatile flash memory stores instructions that result in modification of the operating frequency of the processor and results in adjustment of the operating voltage of the processor [see the Abstract, Fig. 2, and col. 9 lines 41 – 59].

It would have been obvious to one ordinary skilled in the art at the time the invention was made to put Dischler et al.'s table in Clark et al.'s memory so that selectable entries of clock frequency and voltage level would be non-volatile.

16. As per claim 8, it would have been obvious to one ordinary skilled in the art at the time the invention was made to include at least two entries in the table so that there would be entries to choose from in order to achieve efficient processor performance.

17. As per claim 10, Dischler et al. teach a computer system comprising means for selecting the minimum and maximum operable values of clock frequency [col. 8 lines 37 – 43]. Dischler et al. also teach a table containing a plurality of entries to store the maximum and minimum values of clock frequency and the values in between [see Fig. 7 and col. 7 lines 60 – 65]. Thus, Dischler et al. teach a table with selectable entries.

Dischler et al. do not teach a register that has a limit field to specify how many entries are selectable.

However, it is well known in the art to count the entries from a table and record the number in a register.

Therefore, it would have been obvious to one ordinary skilled in the art at the time the invention was made to read the number of selectable entries from Dischler et al.'s table and record the number value in a register so that the value could indicate a limit field to specify how many entries are selectable.

18. As per claim 11, Dischler et al. teach all of claim 9 and 10.

It is well known in the art to set some of the field in a register as read-write field, and to set some other field as read-only field.

Therefore, it would have been obvious to one ordinary skilled in the art at the time the invention was made to set the selection field in the register as a read-write field so that it would be possible to select different entries in the table, and to set the limit field as read-only field so that the choice of selectable entries would be fixed once set by the manufacturer in order to ensure safe performance of the processor.

19. As per claim 15, Clark et al. teach a computer system, wherein a non-volatile flash memory stores instructions that result in modification of the operating frequency of the processor and results in adjustment of the operating voltage of the processor [see the Abstract, Fig. 2, and col. 9 lines 41 – 59].

It would have been obvious to one ordinary skilled in the art at the time the invention was made to put Dischler et al.'s table in Clark et al.'s memory so that selectable entries of clock frequency and voltage level would be non-volatile.

20. As per claim 16, it would have been obvious to one ordinary skilled in the art at the time the invention was made to include at least two entries in the table so that there would be entries to choose from in order to achieve efficient processor performance.

21. As per claim 17, Clark et al. teach a method, comprising:

writing into a selection field of a register[col. 4 lines 11 – 17];

using a content of the selection field to select a clock frequency and voltage level of the processor [col. 4 lines 11 – 31].

Clark et al. do not teach a method using a content of the selection field to select one of a plurality of entries in a table, each entry having a frequency field and a voltage field.

Dischler et al. teach a method using a register to select one of a plurality of entries in a table, each having a frequency field and a voltage field [see col. 7 lines 60 – 65, col. 6 lines 12 – 19, and col. 7 lines 18 – 24].

Therefore, it would have been obvious to one ordinary skilled in the art at the time the invention was made to combine Clark et al.'s method with Dischler et al.'s method so that selection field in the register can be changed and the selection field can change clock frequency and voltage of the processor by using an entry in the table.

22. As per claims 18 – 25, since they recite the methods necessary to utilize the apparatus defined in the apparatus claims, they are rejected based on the rejection of the apparatus claims.

23. As per claim 26, Clark et al. teach a machine-readable medium having stored thereon instructions, which when executed by a processor cause said processor to perform [see Abstract]:

determining a desired combination of processor clock frequency and processor operating voltage [see Abstract]; and

writing to a register to select the desired combination of processor clock frequency and processor operating voltage [col. 4 lines 11 – 31].

Clark et al. do not teach a device that writes to a register to select the desired combination of processor clock frequency and processor operating voltage from a table.

Dischler et al. teach a device that writes to a register to select the desired combination of processor clock frequency and processor operating voltage from a table [see col. 7 lines 60 – 65, col. 6 lines 12 – 19, and col. 7 lines 18 – 24].

Therefore, it would have been obvious to one ordinary skilled in the art at the time the invention was made to combine Clark et al.'s device with Dischler et al.'s device so that instructions stored in a machine-readable medium would write to a register to determine processor clock frequency and operating voltage based on a table.

24. As per claim 27, Clark et al. teach a register which has a field that can store the current combination of processor clock frequency and processor operating voltage [col.4 liens 11 – 18].

Setting the field of a register readable is well known in the art.

Therefore, it would have been obvious to one ordinary skilled in the art at the time the invention was made to modify Clark et al.'s register so that the medium can read from the register to determine the current combination of processor clock frequency and processor operating voltage.

25. As per claim 28, Dischler et al. teach an apparatus comprising means for selecting the minimum and maximum operable values of clock frequency [col. 8 lines 37 – 43]. Dischler et al. also teach a table containing a plurality of entries to store the maximum and minimum values of clock frequency and the values in between [see Fig. 7 and col. 7 lines 60 – 65]. Thus, Dischler et al. teach a table with selectable entries.

Dischler et al. do not teach a register that has a limit field to specify how many entries are selectable.

However, it is well known in the art to count the entries from a table and record the number in a register. And it is also well known in the art to read the value stored in such a register.

Therefore, it would have been obvious to one ordinary skilled in the art at the time the invention was made to read the number of selectable entries from Dischler et al's table, record the number value in a register, and read the value from the register so that it would be possible to determine how many combinations of processor clock frequency and processor operating voltage are available to be selected.

26. As per claim 29, Clark et al. teach a medium, wherein:

determining a desired combination is based on at least one of:

a performance goal;

a power consumption goal; and

operating characteristics of the processor [see Background].

operating characteristics of the processor [see Background].

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chi Whan Chung whose telephone number is (703)305-8788. The examiner can normally be reached on Monday~Friday 8:30am -4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703)305-9717. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

C.C.

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